3AL82023AA-AO

Alcatel-Lucent Nokia® 3AL82023AA Compatible TAA 100GBase-LR4 CFP4 Transceiver (SMF, 1310nm, 10km, LC, DOM)

Features

- CFP MSA 1.1 Compliance
- Duplex LC Connector
- Commercial Temperature 0 to 70 Celsius
- Single-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead Free

Applications

- 100GBase Ethernet
- Access and Enterprise

Product Description

This Alcatel-Lucent Nokia® 3AL82023AA compatible CFP4 transceiver provides 100GBase-LR4 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1310nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Alcatel-Lucent Nokia® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

Rev. 021022

Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883E Method 3015.4
- ESD to the LC Receptacle: compatible with IEC 61000-4-3
- EMI/EMC compatible with FCC Part 15 Subpart B Rules, EN55022:2010
- Laser Eye Safety compatible with FDA 21CFR, EN60950-1& EN (IEC) 60825-1,2
- RoHS compliant with EU RoHS 2.0 directive 2015/863/EU

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	TS	-40		+85	°C	
Power Supply Voltage	VCC	0		+3.6	V	+3.3V
Operating Case Temperature Range	Tc	0	25	70	°C	
Optical Receiver Input	Pimax			+5.5	dBm	Average
Power Supply Noise	Vrip			2 3	% %	DC – 1MHz 1 – 10MHz

Optical Characteristics (Note 1)

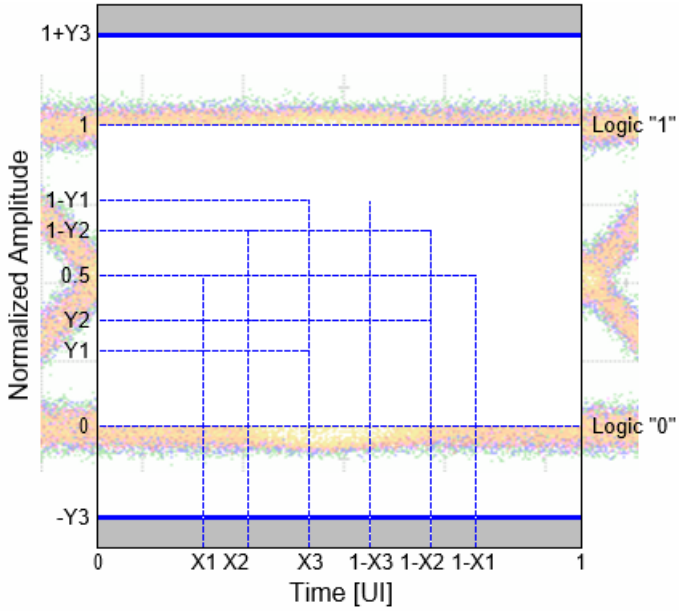
Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter							
Channel data rate		fDC		25.78125		Gbit/s	2
Aggregate data rate		fD		103.125		Gbit/s	2
Signal speed variation from nominal		∆fD	-100		+100	ppm	2
Optical Center Wavelength	**Lane 0**	λ_{CT0}	1294.53		1296.59	nm	
	Lane 1	λ_{CT1}	1299.02		1301.09	nm	
	Lane 2	λ_{CT2}	1303.54		1305.63	nm	
	Lane 3	λ_{CT3}	1308.09		1310.19	nm	
Optical Output Power in OMA		OMA	-1.3		+4.5	dBm	3
Average Optical Output Power of Off Transmitter		Poff			-30	dBm	
Optical Waveform				Eye Diagram			2
Extinction Ratio		ER	4			dB	
Receiver							
Receiver Sensitivity in OMA		PminOMA	-8.6		+4.5	dBm	
Stressed Receiver Sensitivity in OMA		PminSOMA			-6.8	dBm	4
Receive Power, each lane in OMA					+4.5	dBm	

Notes:

1. Data Rate; NRZ, Mark Ratio 50%, PRBS=2^{31}-1, 1x10^{-12} BER unless otherwise specified.
2. Per IEEE 802.3ba specification

3. OMA=$10\log_{10}[2P\{(A-1)/(A+1)\}]$, $A = 10^{(ER/10)}$, $P = 10^{(Pf/10)}$
4. Stressed Receiver Sensitivity measurement method is under study

Mask of Optical Output Eye Diagram



X1	X2	X3	Y1	Y2	Y3	Max hit ratio (Note)
0.25	0.4	0.45	0.25	0.28	0.4	5×10^{-5}

Note:

The acceptable ratio of samples inside to outside the hatched area (the “hit ratio”) must be met.

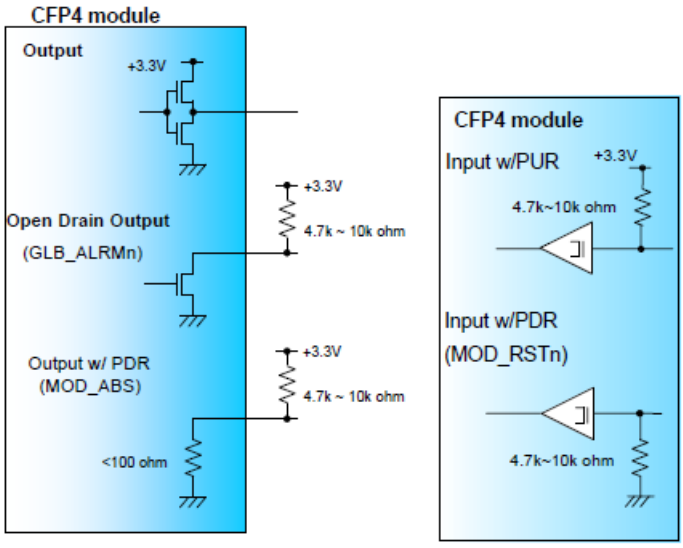
Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	VCC	3.2	3.3	3.4	V	
Supply Current	ICC			1.9	A	1
Supply Current @Low Power Mode	ICCL			0.3	A	
Power Consumption	P			6	W	
Power Consumption @Low Power Mode	Plow			1	W	
3.3V LVCMOS level						
Input High Voltage	VIH	2		VCC + 0.3	V	
Input Low Voltage	VIL	-0.3		0.8	V	
Input Leakage Current	IIN	-10		+10	μA	
Output High Voltage	VOH	VCC – 0.2			V	I_{OH}=-100μA
Output Low Voltage	VOL			0.2	V	I_{OL}=100μA
Minimum Pulse Width of Control Pin Signal	t_CNTL	100				μs
1.2 VLVCMOS Level						
Input High Voltage	VIH	0.84		1.5	V	
Input Low Voltage	VIL	-0.3		0.36	V	
Input Leakage Current	IIN	-100		+100	μA	
Output High Voltage	VOH	1.0		1.5	V	
Output Low Voltage	VOL	-0.3		0.2	V	
Output High Current	IOH			-4	mA	
Output Low Current	IOL	+4			mA	
Input capacitance	Ci			10	pF	

Notes:

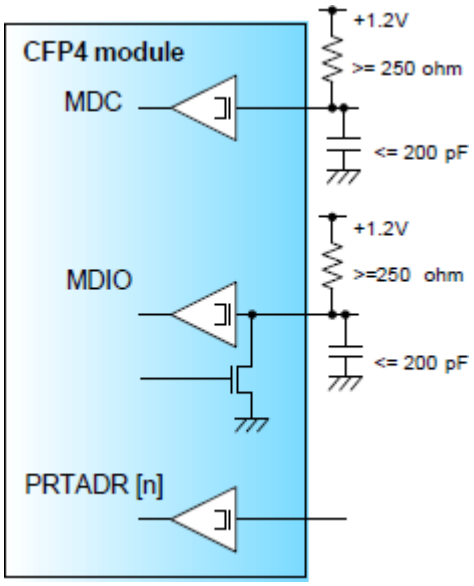
1. Maximum module current ramp rate is 100 mA /μs.

3.3V LVCMOS Interface



MDIO Interface

The below drawings, with maximum host load capacitance of 200pF, also define the measurement set-up for module MDC timing verification. The capacitor in the drawing indicates the stray capacitance on the line. Don't put any physical capacitor on the line.



High Speed Electrical Input Characteristics

Parameter	Symbol	Min.	Max.	Unit	Conditions
Differential Voltage Overload pk-pk	Module Input	900		mV	Calibrated at TP1a
Differential Termination Mismatch	Module Input		10	%	at 1 MHz
Differential Return Loss	Module Input		Note 1	dB	
Common Mode to differential conversion Loss	Host Output	Note 2		dB	

Notes:

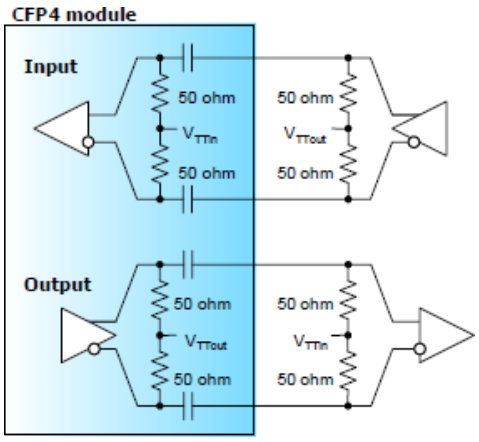
1. SDD11, SDD22 < -11dB for f<fb/7, SDD11, SDD22 < -6.0+9.2*log(2f/fb) dB for fb/7<f<fb (fb=25.78 GHz)
2. SDC11 < -25+20*(f/fb) dB for f<fb/2, SDC11 < -15 dB for fb/2<f<fb (fb=25.78 GHz)

High Speed Electrical Output Characteristics

Parameter	Direction	Min.	Max.	Unit	Conditions
Differential Voltage, pk-pk	Module Output		900	mV	
Common Mode Noise, rms	Module Output		17.5	mV	
Differential Termination Mismatch	Module Output		10	%	at 1 MHz
Differential Return Loss	Module Output		Note 1	dB	
Transition Time: 20/80%	Module Output	9.5		ps	
Vertical Eye Closure (VEC)			6.5	dB	
Eye width at 10-15 probability (EW15)	Module Output	0.57		UI	
Eye height at 10-15 probability (EH15)	Module Output	240		mV	

Notes:

1. SDD11, SDD22 < -11dB for f<fb/7, SDD11, SDD22 < -6.0+9.2*log(2f/fb) dB for fb/7<f<fb (fb=25.78 GHz)



High speed I/O for Data and Clocks

Transmitter & Receiver Monitor Clock Characteristics

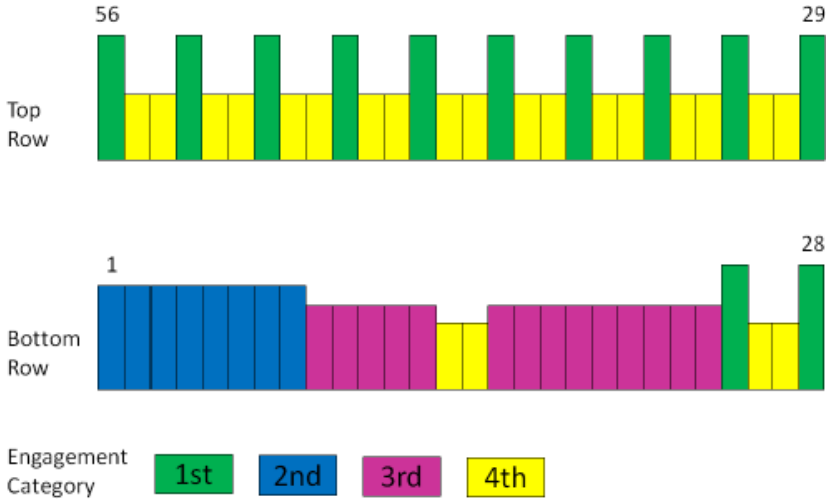
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock Differential Input Impedance	Zd	80	100	120	ohm	
Differential Output Clock Amplitude	V_{DIFF}	400		1200	mVpp	AC coupled CML
Reference Clock Duty Cycle		40		60	%	

Optical signal, Electrical signal, MCLK and REFCLK frequency relation

Parameter	Symbol	Rate	Unit	Remarks
Aggregate data rate	fDC	103.125	Gbit/s	
Optical signal rate per lane (Channel data rate)	fD	25.78125	Gbit/s	$f_{DC}/4$
Electrical signal rate per lane	fhost	25.78125	Gbit/s	
TXMCLK rate	fm	1/8 of network lane rate (3.22266 GHz) or 1/32 of network lane rate (805.665 MHz)		Default: Disabled Note 1
RXMCLK rate	fm	1/8 of network lane rate (3.22266 GHz) or 1/32 of network lane rate (805.665 MHz)		Default: disabled
REFCLK rate	fo	161.1328 ($f_{host}/160$)	MHz	MDIO reg. Selectable

Notes:

1. For optical signal measurement trigger



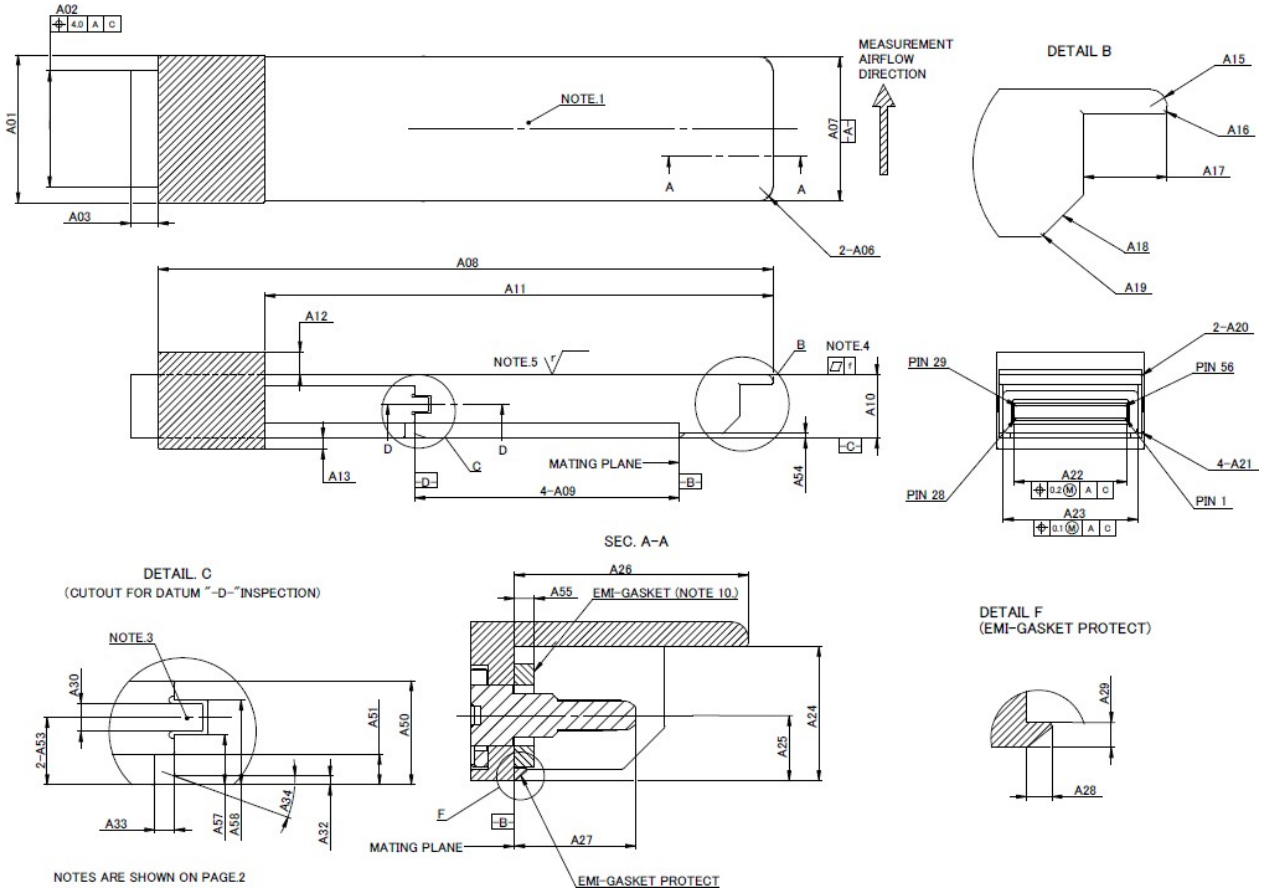
	CFP4 Bottom
1	3.3V_GND
2	3.3V_GND
3	3.3V
4	3.3V
5	3.3V
6	3.3V
7	3.3V_GND
8	3.3V_GND
9	VND_IO_A
10	VND_IO_B
11	TX_DIS *(PRG_CNTL1)*
12	RX_LOS *(PRG_ALRM1)*
13	GLB_ALRMn
14	MOD_LOPWR
15	MOD_ABS
16	MOD_RSTn
17	MDC
18	MDIO
19	PRTADR0
20	PRTADR1
21	PRTADR2
22	VND_IO_C
23	VND_IO_D
24	VND_IO_E
25	GND
26	*(MCLKn)*
27	*(MCLKp)*
28	GND

	CFP4 Top
56	GND
55	TX3n
54	TX3p
53	GND
52	TX2n
51	TX2p
50	GND
49	TX1n
48	TX1p
47	GND
46	TX0n
45	TX0p
44	GND
43	*(REFCLKn)*
42	*(REFCLKp)*
41	GND
40	RX3n
39	RX3p
38	GND
37	RX2n
36	RX2p
35	GND
34	RX1n
33	RX1p
32	GND
31	RX0n
30	RX0p
29	GND

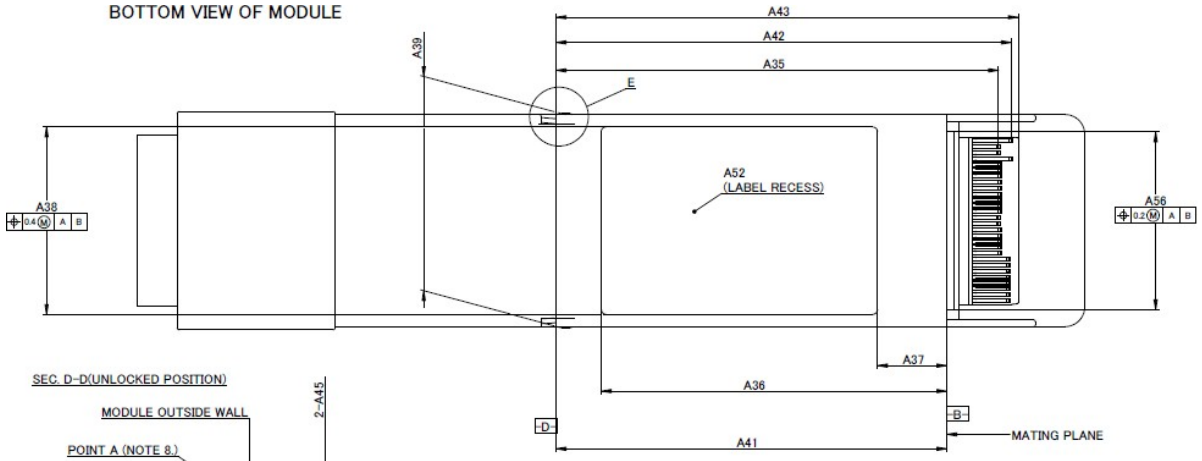
Pin Descriptions

PIN	Name	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separated or tied together with Signal Ground
2	3.3V_GND			
3	3.3V			
4	3.3V			
5	3.3V			
6	3.3V			3.3V Module Supply Voltage
7	3.3V_GND			
8	3.3V_GND			
9	VIND_IO_A	I/O		Module Vendor I/O A. Do Not Connect
10	VIND_IO_B	I/O		Module Vendor I/O B. Do Not Connect
11	TX_DIS (PRG_CNT L1)	I	LVCMOS w/PUR	Transmitter Disable for all lanes. "1" or NC: Transmitter disabled; "0": transmitter enabled. (Optionally configurable as Programmable Control1 after Reset)
12	RX_LOS (PRG_ALR M1)	O	LVCMOS w/PUR	Receiver Loss of Optical Signal. "1": low optical signal; "0": normal condition (Optionally configurable as Programmable Alarm1 after Reset)
13	GLB_ALR M	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register; "1": no alarm condition, Open Drain, Pull up Resistor on Host
14	MOD_LOP WR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode; "0": power-on enabled
15	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent; "0": module present, Pull up resistor on Host
16	MOD_RSTn	I	LVCMOS w/PDR	Module Reset. "0": resets the module; "1" or NC: module enabled, Pull down Resistor in Module
17	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
18	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3ae-2008 and ba-2010)
19	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
20	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
21	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
22	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect
23	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect
24	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect
25	GND			
26	(MCLKn)	O	CML	For optical waveform testing. Not for normal use
27	(MCLKp)	O	CML	For optical waveform testing. Not for normal use
28	GND			

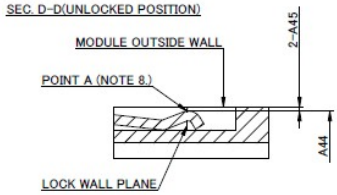
Mechanical Specifications



BOTTOM VIEW OF MODULE

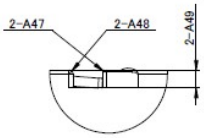


SEC. D-D(UNLOCKED POSITION)

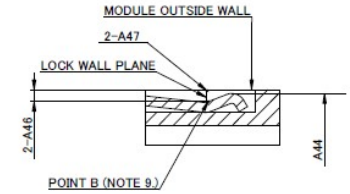


DETAILE

(CUTOUT FOR DATUM "-D-"INSPECTION)



SEC. D-D (LOCKED POSITION)



NOTE

1. 7 deg C MAXIMUM TEMPERATURE DELTA WITH NO HEATSINK AND 200LFM SIDEWAYS AIR FLOW. (DELTA TEMPERATURE SPECIFICATION TO BE VERIFIED WITH FIRST ARTICLES).
2. DRAFT ANGLE TO BE IN THE DECREASING MASS DIRECTION.
3. MODULE LATCH POSITION MUST INTEROPERATE WITH CFP4 CAGE SPECIFICATIONS.
4. SURFACE FLATNESS: "f" IS SPECIFIED IN CFP4 HARDWARE SPECIFICATION.
5. SURFACE ROUGHNESS: "r" IS SPECIFIED IN CFP4 HARDWARE SPECIFICATION.
6. DIMENSION APPLIES TO LATCH MECHANISM.
7. MAXIMUM OUTSIDE ENVELOP BETWEEN TWO OPPOSITE LATCHES.
8. "POINT A" IS AT THE VIRTUAL INTERSECTION OF LOCK WALL PLANE AND OUTER SURFACE OF LATCH.
9. "POINT B" IS AT THE VIRTUAL INTERSECTION OF LOCK WALL PLANE AND OUTER SURFACE OF LATCH.
10. GASKET TO MEET MINIMUM PEELS STRENGTH : 30 Oz/in or 335 gf/cm per ASTM D3330 test method.

About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is in engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

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